IN THE CLAIMS

Claims 1-8 were pending. No claims have been canceled. Claim 5 has been amended. New claims 9-10 have been added without introducing any new matter. Claims 1-10 are currently pending. A complete list of claims is presented below:

Current Listing of Claims

1. (Previously presented) A processor comprising:

a translation-lookaside-buffer (TLB);

a cache to provide temporary storage for a data block; and

a memory management unit to implement a first cache-coherency mechanism or a second cache-coherency mechanism using the TLB according to a property of an operating system to be run by the processor.

2. (Original) The processor of claim 1, wherein the TLB includes a plurality of entries, each entry including a virtual address tag, a physical address, and a memory attribute.

3. (Original) The processor of claim 2, wherein the first cache coherency mechanism snoops the cache if an access to a memory address designated by an uncacheable memory attribute is detected.

4. (Previously presented) A computer system comprising:

an execution core;

a cache having a plurality of data entries;

a memory to store an operating system for the computer system; and

a memory management unit to manage data flow among the execution core, the cache and the memory, the memory management unit to operate in a first cache coherency mode or a second cache coherency mode according to a property of the operating system.

5. (Currently amended) [[The]] A computer system ~~of claim 4~~ comprising:

an execution core;

a cache having a plurality of data entries;

a memory to store an operating system for the computer system; and

a memory management unit to manage data flow among the execution core, the cache and the memory, the memory management unit to operate in a first cache coherency mode or a second cache coherency mode according to a property of the operating system, wherein the first cache coherency mode supports memory attribute aliasing and the second cache coherency mode does not support memory attribute aliasing.

6. (Previously presented) A method comprising:

identifying an operating system to be run on a computer system; and

booting the computer system in a first cache coherency mode or a second cache coherency mode according to a property of the operating system.

7. (Previously presented) The method of claim 6, wherein booting the computer system in the first cache coherency mode comprises configuring a memory management unit to self-snoop a cache in response to selected memory accesses.

8. (Previously presented) The method of claim 6, wherein booting the computer system in the second cache coherency mode comprises configuring a memory management unit to forward selected memory accesses to a cache to detect memory attribute conflicts.

9. (New) The method of claim 6, wherein the first cache coherency mode supports memory attribute aliasing and the second cache coherency mode does not support memory attribute aliasing.

10. (New) The processor of claim 1, wherein the first cache coherency mechanism supports memory attribute aliasing and the second cache coherency mechanism does not support memory attribute aliasing.